Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

IN THE CLAIMS:

1. (Currently amended): A semiconductor device comprising:

an underlie having a conductive region in a surface layer of said underlie;

an insulating etch stopper film covering a surface of said underlie;

an interlayer insulating film formed on said insulating etch stopper film;

a wiring trench formed in said interlayer insulating film, said wiring trench having a bottom surface at a first depth from a surface of said interlayer insulating film, and a side wall;

a contact hole extending from said bottom surface of said wiring trench to a surface of said conductive region through a remaining thickness of said interlayer insulating film and through said insulating etch stopper film; and

a dual damascene wiring layer embedded in said wiring trench and in said contact hole, wherein said interlayer insulating film includes a first kind of an insulating layer surrounding said side wall and said bottom surface of said wiring trench and a second kind of an insulating layer disposed under said first kind of the insulating layer and having etching characteristics different from said first kind of the insulating layer, and

wherein said contact hole has an upper portion whose cross sectional area gradually increases toward an upper level and reaches said bottom surface of said wiring trench in said first kind of the insulating layer and a portion with uniform cross sectional area connected below said upper portion.

2. (Canceled)

3. (Original): A semiconductor device according to claim 1, wherein said interlayer insulating film further includes a third kind of an insulating layer under the second kind of the insulating layer, the third kind of the insulating layer having etching characteristics different from the second kind of the insulating layer.

4. (Previously presented): A semiconductor device according to claim 3, wherein said contact hole has a portion whose cross sectional area gradually increases from an intermediate level of said second kind of the insulating layer toward an upper level and reaches said bottom surface of said wiring trench.

5. (Original): A semiconductor device according to claim 3, wherein the second kind of the insulating layer is capable of functioning as an etch stopper while the first kind of the insulating layer is etched, and said contact hole has a substantially same cross sectional shape from a bottom surface of the second kind of the insulating layer to the surface of the conductive region.

6. (Original): A semiconductor device according to claim 3, wherein the third kind of the insulating layer has a thickness thinner than the first depth.

7. (Original): A semiconductor device according to claim 1, wherein the second kind of the insulating layer is disposed on said insulating etch stopper film and has a thickness thinner than the first depth.

8-18. (Canceled)

19. (Previously presented): A semiconductor device according to claim 1, wherein said interlayer insulating layer has a shoulder at said portion, which extends from said bottom surface into said second kind of the insulating layer.

20. (Previously presented): A semiconductor device according to claim 19, wherein said shoulder is smoothly continuous with the bottom surface.

21. (Previously presented): A semiconductor device according to claim 20, wherein said shoulder is formed by etching from above and from said contact hole.

22. (Previously presented): A semiconductor device according to claim 1, wherein said interlayer insulating film has a rounded shoulder at said portion.

23. (Previously presented): A semiconductor device according to claim 22, wherein said shoulder extends from said bottom surface in said first kind of the insulating layer to an intermediate position of said contact hole in said second kind of the insulating layer.

24. (Previously presented): A semiconductor device according to claim 1, wherein said contact hole has a generally vertical side wall in a lower part, and a gently sloped shoulder in an upper part.

25. (Previously presented): A semiconductor device according to claim 1, wherein said first kind of the insulating layer is made of fluorine-containing silicon oxide, and said second kind of the insulating layer is made of silicon oxide.

26. (Previously presented): A semiconductor device according to claim 3, wherein said first kind of the insulating layer is made of fluorine-containing silicon oxide, said second kind of the insulating layer is made of silicon nitride, and the third kind of the insulating layer is made of fluorine-containing silicon oxide.

27. (Previously presented): A semiconductor device according to claim 1, wherein said underlie comprises a silicon substrate formed with shallow trench isolation defining active regions, CMOS transistors formed in said active regions, each said transistor having an insulated gate electrode on the active region, and source/drain regions formed in the active region on both sides of the gate electrode.

28. (Previously presented): A semiconductor device according to claim 27, wherein said underlie further comprises lower insulating layers formed on said silicon substrate covering said

gate electrodes and said source/drain regions, and at least one wiring layer embedded in said lower insulating layers.

29. (Previously presented): A semiconductor device according to claim 28, wherein said insulating etch stopper film is made of one selected from the group consisting of silicon nitride, silicon oxynitride, and silicon carbide.

30. (Previously presented): A semiconductor device according to claim 29, wherein said first and second kinds of the insulating layers are selected from silicon oxide layers formed under different conditions, silicon oxide layers made from different materials, silicon nitride layers, silicon oxynitride layers, inorganic compound layers, and organic compound layers.

31. (New): A semiconductor device comprising:

an underlie having a conductive region in a surface layer of said underlie;

an insulating etch stopper film covering a surface of said underlie;

an interlayer insulating film formed on said insulating etch stopper film;

a wiring trench formed in said interlayer insulating film, said wiring trench having a bottom surface at a first depth from a surface of said interlayer insulating film, and a side wall;

a contact hole extending from said bottom surface of said wiring trench to a surface of said conductive region through a remaining thickness of said interlayer insulating film and through said insulating etch stopper film; and

a dual damascene wiring layer embedded in said wiring trench and in said contact hole,

wherein said interlayer insulating film includes a first kind of an insulating layer surrounding said side wall and said bottom surface of said wiring trench and a second kind of an insulating layer disposed under said first kind of the insulating layer and having etching characteristics different from said first kind of the insulating layer, and

wherein said contact hole has an upper portion in said first kind of the insulating layer, a cross sectional area of said upper portion gradually increases toward an upper level and reaches said bottom surface of said wiring trench in said first kind of the insulating layer.

32. (New): A semiconductor device according to claim 31, wherein said first kind of the insulating layer is made of fluorine-containing silicon oxide, and said second kind of the insulating layer is made of silicon oxide.

33. (New): A semiconductor device according to claim 31, wherein said underlie comprises a silicon substrate formed with shallow trench isolation defining active regions, CMOS transistors formed in said active regions, each said transistor having an insulated gate electrode on the active region, and source/drain regions formed in the active region on both sides of the gate electrode.

34. (New): A semiconductor device according to claim 33, wherein said underlie further comprises lower insulating layers formed on said silicon substrate covering said gate electrodes and said source/drain regions, and at least one wiring layer embedded in said lower insulating layers.

35. (New): A semiconductor device according to claim 34, wherein said insulating etch stopper film is made of one selected from the group consisting of silicon nitride, silicon oxynitride, and silicon carbide.

36. (New): A semiconductor device according to claim 35, wherein said first and second kinds of the insulating layers are selected from silicon oxide layers formed under different conditions, silicon oxide layers made from different materials, silicon nitride layers, silicon oxynitride layers, inorganic compound layers, and organic compound layers.